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202EC008

Ph.D./M.S. (Engg.) by Research Degree Examination, December 2022
Advances in VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain semi custom design flow. **(10 Marks)**

b. What are premised arrays? Explain their classification. **(10 Marks)**

OR

2 a. Explain programmable logic in pre-wired arrays. **(10 Marks)**

b. Differentiate between array and mesh interconnect architectures. **(10 Marks)**

Module-2

3 a. What is cross talk? Describe capacitive cross talk on floating lines and driven lines. How to deal with capacitive cross talks. **(12 Marks)**

b. Explain impact of cross talk on delay. How to reduce delay effects. **(08 Marks)**

OR

4 a. What is Electromigration? Explain Electro migration related failure modes. **(07 Marks)**

b. Explain the Global Wire problem. **(05 Marks)**

c. What are the design techniques to address $h\left(\frac{di}{dt}\right)$ problem? Explain. **(08 Marks)**

Module-3

5 a. Explain the impact of clock skew and jitter on performance. Also explain the sources of skew and jitter. **(10 Marks)**

b. Compare synchronous pipelined datapath with self timed pipelined datapath. **(10 Marks)**

OR

6 a. Explain Muller C-element implementation for dynamic circuit realization. Also explain how Muller C-element implements a Z – phase handshake protocol. **(10 Marks)**

b. Explain clock synthesis using phase – locked loop. **(10 Marks)**

Module-4

7 a. Explain Array structured memory architecture. **(08 Marks)**

b. Explain contents – Address able memory. **(08 Marks)**

c. Explain memory timing approaches. **(04 Marks)**

OR

8 a. Explain basic operations in NOR Flash Memory – Erase, Write and Read. **(10 Marks)**

b. Explain differential sense amplifier in SRAM sensing scheme. **(10 Marks)**

Module-5

9 a. Explain noise sources in 1T DRAM. **(06 Marks)**

b. Explain transposed – Bittine architecture. **(06 Marks)**

c. Explain the sources of power dissipation in memories. **(08 Marks)**

OR

10 a. How leakage in SRAM is suppressed? **(06 Marks)**

b. Explain relation between redundancy and error correction with yield. **(06 Marks)**

c. Explain 4M bit SARM Hierarchical word – line architecture. **(08 Marks)**

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