CBCS SCHEME

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20EVE21

Second Semester M.Tech. Degree Examination, Dec.2023/Jan.2024
Design of Analog and Mixed VLSI Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the operation of common source stage with resistive load and diode load. **(10 Marks)**
b. Explain the operation of folded cascade amplifier. **(10 Marks)**

OR

2 a. Derive expression for the tranconductance of a MOSFET as a function of over drive and drain circuit and plot the variation. **(10 Marks)**
b. Draw the complete small signal model of a MOSFET and label all components. **(10 Marks)**

Module-2

3 a. With neat circuit diagrams, explain the operation of Gilbert cell. **(10 Marks)**
b. With neat circuit diagrams and explain the operation of cascade current mirrors. **(10 Marks)**

OR

4 a. Using equivalent circuit approach derive an expression for the voltage gain of source follower. **(10 Marks)**
b. Give the circuit of a folded cascade stage with pros input transistor and obtain its large signal characteristics V_{out} versus V_{in}. **(10 Marks)**

Module-3

5 a. Draw the small signal model of differential amplifier, using this model obtain the expression for A_v and r_{out}. **(10 Marks)**
b. Describe in steps the design procedure of unbuffered op-amp circuit. **(10 Marks)**

OR

6 a. Design and explain procedure for the two stage CMOS op-amp. **(10 Marks)**
b. Discuss in detail the compensation of op-amp. **(10 Marks)**

Module-4

7 a. Explain the working of a charge pump PLL with relevant circuit diagram and waveforms. **(10 Marks)**
b. Explain in detail the various non-ideal effects of PLL. **(10 Marks)**

OR

8 a. Derive an expression for negative PSRR. **(10 Marks)**
b. Explain common mode feedback and slew rate. **(10 Marks)**

Module-5

9 a. Explain in detail with a neat diagram, successive approximation – ADC. **(10 Marks)**
b. Explain the R – 2R DAC. **(10 Marks)**

OR

10 a. Draw the circuit of parallel ADC and explain its working. **(10 Marks)**
b. Explain the construction and working of delta–sigma ($\Delta\Sigma$) modulator with the help of block diagram. **(10 Marks)**

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