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10EE764

Seventh Semester B.E. Degree Examination, Dec.2023/Jan.2024
VLS Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the process of nMOS fabrication with neat diagrams. **(10 Marks)**
b. Discuss Moore's law with graph. **(04 Marks)**
c. Compare CMOS and Bipolar technology. **(06 Marks)**

2 a. Explain CMOS inverter operation. Draw its transfer characteristics and mark five regions of operation. Also explain the status of nMOS and PMOS transistor in each region. **(08 Marks)**
b. Derive an expression for the drain to source current(I_{ds}) in the region i) linear ii) saturation for the enhancement mode nMOS transistor. **(07 Marks)**
c. Explain latch-up phenomenon in CMOS VLSI. Also discuss its remedies. **(05 Marks)**

3 a. Explain Lambda based design rules for wires and minimize size transistors. **(10 Marks)**
b. Explain buried and butting contract with neat diagram. **(06 Marks)**
c. Draw the circuit and stick diagram for CMOS inverter. **(04 Marks)**

4 a. Derive an expression for rise time (t_r) and fall time (t_f) for CMOS inverter. Is $t_r = t_f$? If not, deduce the condition to make $t_r = t_f$. **(10 Marks)**
b. Derive an expression for total delay for N stages of nMOs and CMOS inverters in terms of width factor 'f' and delay 's' while driving a large capacitive load C_L. **(10 Marks)**

PART - B

5 a. Derive scaling factor for any ten device parameters. **(10 Marks)**
b. Discuss the limitation of scaling on interconnect and contact resistance. **(10 Marks)**

6 a. Discuss the architectural issues in the VLSI subsystem design. **(06 Marks)**
b. What are pass gates? What are its properties? How is transmission gate useful? **(06 Marks)**
c. Explain the principles of structured design approach with the help of parity generator. **(08 Marks)**

7 a. Explain the operation of 4 × 4 barrel shifter. **(10 Marks)**
b. Explain the general arrangement of 4-bit arithmetic processor. **(06 Marks)**
c. List the general considerations for VLSI design. **(04 Marks)**

8 a. Explain implementation of ALU functions with an adder using appropriate figures and expressions. **(10 Marks)**
b. Draw the structure of multiplexer based adder logic with stored and buffered sum output and explain. **(10 Marks)**

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